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Appeal Brief Under 37 C.F.R. §41.37 (25 sheets)
Appendix A (4 sheets)
Appendix B (1 sheet)
Appendix C (1 sheet)

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Confirmation No.:	5374	Examiner:	Vu, Tuan A.
Filing Date:	26 October 2000	Inventor:	McNutt, Alan

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12 Jun 2006	Eden Brown	Eden Brown
Date	Name of Certifier	Signature of Certifier

PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Alan D. McNutt
Application #	:	09/697,419
Confirmation #	:	5374
Filed	:	26 October 2000
Application Title	:	RE-PROGRAMMABLE FLASH MEMORY MICRO CONTROLLER AS PROGRAMMABLE LOGIC CONTROLLER
Art Unit #	:	2124
Latest Examiner	:	Tuan A. Vu
Docket No.	:	1999P07938US01 (1009-045)

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APPEAL BRIEF UNDER 37 C.F.R. §41.37

Sir:

Applicant respectfully submits this Appeal Brief in response to a Final Office Action of 27 June 2005 ("the Final Office Action") finally rejecting each of the pending claims 4-11, in response to an Office Action of 5 April 2006 ("the present Office Action") in which prosecution was reopened, and in furtherance of the Notice of Appeal filed 5 June 2006. Applicant respectfully requests that the fees paid with the Appeal Brief filed on 26 December 2006 be applied to the fees due for the attached Appeal Brief.

I. REAL PARTY IN INTEREST

The real party in interest is Siemens Energy & Automation, Inc., a corporation having a place of business at 3333 Old Milton Parkway, Alpharetta, GA 30005.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3 were cancelled. Claims 4-11 are pending in this application, have been finally rejected, and are the subject of this appeal. Each of claims 4, 5, 7, 9, and 11 are in independent form.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 4

Independent claim 4 recites an apparatus (*see* at least page 5, lines 23-29; Figure 1 Program Execution Device) that comprises a programmable logic controller lacking instructions to convert a user program from a symbolic form to a binary form (*see* at least page 5, lines 5-8). The programmable logic controller comprises a single chip program execution device (*see* at least page 5, lines 23-29; Figure 1 Program Execution Device). The single chip program execution device comprises a micro controller (*see* at least page 3, lines 23-29; Figure 1 micro controller 10) operable to implement programmable logic controller I/O functions upon executing a compilation comprising the user program and a system support kernel (*see* at least page 4, lines 1-8). The system support kernel is adapted to provide the programmable logic controller with operating system functions comprising sequencing the user program (*see* at least page 4, lines 10-14). The apparatus also comprises a re-programmable read only memory within

which the compilation is stored (*see* at least page 5, lines 23-29; Figure 1 reprogrammable Flash EEPROM 16). The single chip program execution device is separable from a communication/programming device adapted to convert the user program to a binary code module and combine the binary code module with the system support kernel into a single executable firmware module (*see* at least page 5, lines 23-29). The programmable logic controller lacks a memory device external to the chip program execution device (*see* at least Figure 1).

Independent Claim 5

Independent claim 5 recites a method that comprises receiving a symbolic user program at a communication/programming device (*see* at least page 4, lines 1-8). The communication/programming device is separable from a single chip program execution device having a re-programmable read only memory (*see* at least page 5, lines 23-29). The single chip program execution device is adapted to execute a binary programmable logic control program (*see* at least page 4, lines 1-8). The binary programmable logic control program is stored within the re-programmable memory (*see* at least page 6, lines 1-8). The binary programmable logic control program is adapted to operate a programmable logic controller (*see* at least page 4, lines 1-8). The programmable logic controller lacks a memory device external to the single chip program execution device (*see* at least page 5, lines 4-8). The method also comprises compiling, at the communication/programming device, the symbolic user program with a system support kernel to form the binary programmable logic control program (*see* at least page 4, lines 10-14). The system support kernel is adapted to provide the programmable logic controller with operating system functions comprising sequencing the user program (*see* at least page 4, lines 10-14).

Dependent Claim 6

To independent claim 5, claim 6 adds that the method also comprises providing the binary programmable logic control program to the single chip program execution device (*see* at least page 4, lines 1-8).

Independent Claim 7

Independent claim 7 recites a method that comprises receiving, from a communication/programming device (*see* at least page 4, lines 1-8; Figure 1 Program Execution Device), a binary programmable logic control program at a single chip program execution device having a re-programmable read only memory (*see* at least page 4, lines 1-8). The communication/programming device is separable from the single chip program execution device (*see* at least page 5, lines 17-21). The binary programmable logic control program comprises a compilation of a symbolic user program combined with a system support kernel to form a single executable module (*see* at least page 4, lines 1-8). The system support kernel is adapted to provide a programmable logic controller with operating system functions comprising sequencing the user program (*see* at least page 4, lines 1-8). The single chip program execution device is adapted to execute the binary programmable logic control program to operate a programmable logic controller (*see* at least page 4, lines 1-8). The programmable logic controller lacks a memory device external to the single chip program execution device (*see* at least page 5, lines 4-8). The method also comprises loading the binary programmable logic control program into the re-programmable read only memory of the program single chip execution device (*see* at least page 4, lines 1-8).

Dependent Claim 8

To independent claim 7, claim 8 adds that the method also comprises executing the binary programmable logic control program on a micro controller of the single chip program execution device (*see* at least page 4, lines 1-8).

Independent Claim 9

Independent claim 9 recites a programmable logic controller system (*see* at least Figure 1) that comprises within a single chip, a program execution device having a re-programmable memory (*see* at least page 5, lines 23-29; Figure 1 Program Execution Device). The program execution device is adapted to execute a binary programmable logic control program (*see* at least page 4, lines 1-8). The binary programmable logic control program is stored within the re-programmable memory (*see* at least page 6, lines 1-8). The binary programmable logic control

program comprises a compilation of a user program and a system support kernel (*see* at least page 4, lines 10-14). The binary programmable logic control program is adapted to operate a programmable logic controller (*see* at least page 4, lines 1-8). The programmable logic controller lacks a memory device external to the single chip program execution device (*see* at least page 5, lines 4-8). The programmable logic controller system also comprises a communication/programming device separable from the program execution device (*see* at least page 5, lines 23-29). The communication/programming device provides functions required for external communication of the binary programmable logic control program (*see* at least page 4, lines 1-8). The binary programmable logic control program comprises a binary module formed from compiling a symbolic user program (*see* at least page 6, lines 1-8). The binary module is combined with a system support kernel to form a single executable module (*see* at least page 6, lines 10-14). The system support kernel is adapted to provide the programmable logic controller with operating system functions comprising sequencing the user program (*see* at least page 6, lines 10-14). The communication/programming device is adapted to load the binary programmable logic control program into the re-programmable memory (*see* at least page 4, lines 1-8). The binary programmable logic control program is stored in the re-programmable memory of the program execution device by direct manipulation of logic controls of the re-programmable memory (*see* at least page 4, lines 1-8).

Dependent Claim 10

To independent claim 9, claim 10 adds that the programmable logic controller system also comprises a watchdog timer (*see* at least page 6, lines 10-14).

Independent Claim 11

Independent claim 11 recites a machine-readable medium storing instructions for activities that comprise receiving a symbolic user program at a communication/programming device (*see* at least page 4, lines 1-8). The communication/programming device is separable from a single chip program execution device having a re-programmable read only memory (*see* at least page 5, lines 23-29). The single chip program execution device is adapted to execute a binary programmable logic control program (*see* at least page 4, lines 1-8). The binary programmable

logic control program is stored within the re-programmable memory (*see* at least page 6, lines 1-8). The binary programmable logic control program is adapted to operate a programmable logic controller (*see* at least page 4, lines 1-8). The binary programmable logic control program comprises a binary module derived via compiling a symbolic user program (*see* at least page 6, lines 1-8). The binary module combined with a system support kernel to form a single executable module (*see* at least page 6, lines 10-14). The system support kernel is adapted to provide the programmable logic controller with operating system functions comprising sequencing the user program (*see* at least page 6, lines 10-14). The programmable logic controller lacks a memory device external to the single chip program execution device (*see* at least page 5, lines 4-8). The activities also comprise compiling, at the communication/programming device, the symbolic user program with a system support kernel to form the binary programmable logic control program (*see* at least page 4, lines 1-8).

VI. GROUNDS OF REJECTION

Claims 4-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Webb et al., "Programmable Logic Controllers – Principles and Applications", 3rd Ed., Prentice Hall, 1995 ISBN: 002429807 (Webb) in view of U.S. Patent No. 4,485,455 (Boone).

VII. ARGUMENT

A. General Legal Standards for Obviousness

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Federal Circuit law further mandates that references "that teach away cannot serve to create a *prima facie* case of obviousness." *See*, In re Gurley, 27 F.3d 551, 553, 31 U.S.P.Q.2D (BNA) 1130, 1132 (Fed. Cir. 1994). If a proposed combination would render a reference

inoperable for its intended purpose, the reference teaches away from the proposed combination. *Tec Air, Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 52 USPQ2d 1294 (Fed. Cir. 1994). "If references taken in combination would produce a 'seemingly inoperative device,'... such references teach away from the combination and thus cannot serve as predicates for a *prima facie* case of obviousness". *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 60 USPQ2d 1001, 1010 (Fed. Cir. 2001).

B. Enablement

"In order to render a claimed apparatus or method obvious, the prior art must **enable** one skilled in the art to make and use the apparatus or method." *Rockwell Int'l Corp. v. U.S.*, 147 F.2d 1358, 47 USPQ2d 1027 (Fed. Cir. 1998); *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1471, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997); *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551, 13 USPQ2d 1301, 1304 (Fed. Cir. 1989).

C. Inoperative Combination

It is inappropriate to combine references when the combination "would produce a seemingly inoperative device." *See, Nat's Steel Car, Ltd. v. Canadian Pac. Ry., Ltd.*, 357 F.3d 1319, 1339 (Fed. Cir. 2004); *Tec Air Inc. v. Denso Mfg. Mich. Inc.*, 192 F.3d 1353, 1360 (Fed. Cir. 1999) (*quoting In re Sponnoble*, 405 F.2d 578, 587 (CCPA 1969).

D. Motivation or Suggestion to Combine the Applied References

"The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness." MPEP 2142. The requirements for fulfilling this burden are explicit and straightforward.

"[T]he examiner **must show reasons** that the skilled artisan, **confronted with the same problems** as the inventor and with no knowledge of the claimed invention, **would select the elements** from the cited prior art references for combination **in the manner claimed.**" (emphasis added). *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998). To show these reasons, "[p]articular findings must be made". *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). Such factual findings must be supported by "concrete

evidence in the record". *In re Zurko*, 258 F.3d 1379, 1385-86, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001).

Moreover, a showing of combinability must be "clear and particular". *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 161(Fed. Cir. 1999). That strong showing is needed because, **"obviousness requires proof** 'that the skilled artisan . . . would select the elements from the cited prior art references for combination in the manner claimed'". *In re Johnston*, 435 F.3d 1381 (Fed. Cir. 2006) (quotation omitted) (emphasis added).

Consequently, an Office Action must clearly and objectively prove that the applied references are "reasonably pertinent to the **particular** problem with which the invention was involved". *See Rutz v. A.B. Chance Co.*, 234 F.3d 654, 664, 57 USPQ2d 1161, 1166 (Fed. Cir. 2000); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1535, 218 USPQ 871, 876 (Fed. Cir. 1983); and *Monarch Knitting Machinery Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 881-83, 886, 45 USPQ2d 1977, 1981-82, 1985 (Fed. Cir. 1998).

In addition, "[t]he patent examination process centers on prior art and the analysis thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness." *In re Sang-Su Lee*, 277 F.3d 1338, 1342, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Thus, the Office Action must clearly and objectively prove some "suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to":

"select the references";

"select the teachings of [the] separate references"; and

"combine [those teachings] in the way that would produce the claimed invention".

In re Johnston, 435 F.3d 1381 (Fed. Cir. 2006) (internal citations omitted). *See also In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (discussing the "the test of whether it would have been obvious to select **specific** teachings and combine them as did the applicant") (emphasis added); and *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985) ("When prior art references require selective combination... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself."). "The absence of . . . a

suggestion to combine is dispositive in an obviousness determination." *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997).

Further, this obviousness standard applies regardless of whether the Office Action relies upon modifying or combining purported teachings.

> Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious modification of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the **desirability** of the modification.... It is impermissible to use the claimed invention as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecated the claimed invention.
>
> *In re Fritch*, 972 F.2d 1260, 23 USPQ 2d 1780, 1783-1784 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985); and *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988) (internal quotations omitted) (emphasis added)).

Therefore, the Office Action also must clearly and objectively prove that the "prior art suggested the **desirability**" of that modification or combination. *See also Akamai Techs. v. Cable & Wireless Internet Servs.*, 344 F.3d 1186, 68 USPQ 2d 1186 (Fed. Cir. 2003) ("[w]hen determining the patentability of a claimed invention which combines two known elements, the question is whether there is something in the prior art as a whole to suggest the **desirability**, and thus the obviousness, of making the combination.") (emphasis added).

E. Claim 4

1. Missing Elements

Claim 4 recites *inter alia*, yet the present Office Action fails to even allege that the relied upon references teach, "a programmable logic controller lacking instructions to convert a user program from a symbolic form to a binary form".

Claim 4 recites *inter alia*, yet the applied portion of Webb does not teach, "executing a compilation comprising a user program and a system support kernel". Instead, the applied portion of Webb allegedly recites (best available image from copy supplied by USPTO):

CHIP	FIXED (F) OR ALTERABLE (A)	APPLICATION	ERASABLE BY
ROM	F	[illegible]	No
RAM	A	User Program	No
PROM	F	User Program	No
EPROM	A	User Program	UV Light
EEPROM	A	User Program	Electrical Signals
NOVRAM	A	User Program	Electrical Signals

FIGURE 3-8
Major Types of IC Memory Chips Used in PLC CPUs

Applicant respectfully asks:

a.) where is the claimed "system support kernel"?

b.) where is the claimed "compilation comprising a user program and a system support kernel"?

c.) where is the claimed "executing a compilation comprising a user program and a system support kernel"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not cure the deficiencies of Webb.

Claim 4 recites *inter alia*, yet the applied portion of Webb does not teach, "a communication/programming device adapted to convert the user program to a binary code module and **combine the binary code module with the system support kernel into a single executable firmware module**". The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach "a communication/programming device

adapted to convert the user program to a binary code module and **combine the binary code module with the system support kernel into a single executable firmware module**"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not overcome the deficiencies of Webb.

Thus, even if there were motivation or suggestion to modify or combine the cited portions of the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the cited portions of the applied references (another assumption with which the applicant disagrees), the combined cited portions of the applied references still do not expressly or inherently teach or suggest every limitation of the independent claims, and consequently fail to establish a *prima facie* case of obviousness with respect to claim 4. Consequently, Applicant respectfully requests reversal of the rejection of claim 4.

2. An Inoperative Combination Would Result from Combining Webb with Boone

Claim 4 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". In order to overcome the deficiencies of Webb, the present Office Action proposes a combination with Boone. Yet claim 4 recites *inter alia*, "a re-programmable read only memory within which the compilation is stored". Webb requires a "random access" or "reprogrammable memory" to store, *inter alia*, "the ladder logic program", "information needed to carry out the user program", "the status of discrete input and output devices", "the preset and accumulated values of counters and timers", "internal I/O relay equivalents", "timer status" values, "counter status" values, and "numerical data". *See* at least page 32 of Webb. However, the calculator of Boone only comprises ROM memory. *See* e.g., ROM 208 of FIG. 2. Regarding this memory, Boone allegedly recites "**programmable read only memory** and the programmable logic arrays are easily **modified by changing only the gate-insulator mask for the metal-insulator-semiconductor integrated system embodiment during the fabrication process**." *See* col. 2, lines 6-11.

Applicant respectfully submits that placing the single chip "calculator" of Boone in the "programmable logic controller" of Webb would result in a device that would be inoperative for programmable logic controller functionality due to a lack of either random access memory or

reprogrammable memory.

Accordingly, Applicant respectfully submits "[i]t is inappropriate to combine" Webb and Boone since the combination "would produce a seemingly inoperative device." Accordingly, the present Office Action fails to establish a *prima facie* case of obviousness regarding claim 4. Consequently, Applicant respectfully requests reversal of the rejection of claim 4.

3. Enablement of References

Claim 4 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". Applicant respectfully submits that neither Webb nor Boone enable a "single chip program execution device" that comprises all of the limitations of claim 4. Consequently, Applicant respectfully requests reversal of the rejection of claim 4.

4. Legally Insufficient Suggestion or Motivation to Combine Webb with Boone

The present Office Action presents a legally insufficient suggestion or motivation to combine Webb with Boone. Regarding this combination, the present Office Action asserts, at page 4:

> [b]ased on Webb's CPU paradigm, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Webb's CPU in a single-chip as taught by Boone because this single-chip would incorporate in one monolithic structure programmable and alterable control logic and storage thereof and processing and control functionalities, thus providing flexible possibilities for code customization while minimizing connections that would otherwise be required to implement all the interfacing pertinent to said functionalities (*see* Boone: col. 1 line 36 to col. 2, line 57).

As an initial matter, applicant points out that Boone has only a "ROM". Accordingly, the calculator of Boone could not "incorporate in one monolithic structure programmable and **alterable** control logic and **storage** thereof" as asserted by the present Office Action. Moreover, Applicant respectfully asks where does this relied upon portion of Boone provide one skilled in the art with any suggestion or motivation to:

a.) "select the references"?

b.) "select the teachings of [the] separate references"?

c.) "combine [those teachings] in the way that would produce the claimed invention"?

Applicant respectfully submits that the relied upon portion of Boone does not provide a legally sufficient suggestion or motivation to combine Boone with Webb. Consequently, Applicant respectfully requests reversal of the rejection of claim 4.

F. Claims 5 and 6

1. Missing Elements

Claim 5, upon which claim 6 depends, recites *inter alia*, yet the applied portions of Webb fail to teach, "compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program." Yet the portions of Webb applied by the present Office Action to reject claim 5 do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach, "compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not overcome the deficiencies of Webb.

Thus, even if there were motivation or suggestion to modify or combine the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the applied references (another assumption with which the applicant disagrees), the combined applied references still do not expressly or inherently teach or suggest every limitation of claims 5 or 6. Consequently, Applicant respectfully requests reversal of the rejection of claims 5 and 6.

2. An Inoperative Combination Would Result From Combining Webb with Boone

Claim 5 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". In order to overcome the deficiencies of Webb, the present Office Action proposes a combination with Boone. Yet claim 5 recites *inter alia*, "a re-

programmable read only memory" in which a "binary programmable logic control program" is stored. Webb requires a random access or reprogrammable memory to store, *inter alia*, "the ladder logic program", "information needed to carry out the user program", "the status of discrete input and output devices", "the preset and accumulated values of counters and timers", "internal I/O relay equivalents", "timer status" values, "counter status" values, and "numerical data". *See* at least page 32 of Webb. However, the calculator of Boone only comprises ROM memory. *See* e.g., ROM 208 of FIG. 2. Regarding this memory, Boone allegedly recites **"programmable read only memory** and the programmable logic arrays **are** easily **modified by changing only the gate-insulator mask for the metal-insulator-semiconductor integrated system embodiment during the fabrication process."** *See* col. 2, lines 6-11.

Applicant respectfully submits that placing the single chip "calculator" of Boone in the "programmable logic controller" of Webb would result in a device that would be inoperative for programmable logic controller functionality due to a lack of either random access memory or reprogrammable memory.

Accordingly, Applicant respectfully submits "[i]t is inappropriate to combine" Webb and Boone since the combination "would produce a seemingly inoperative device." Accordingly, the present Office Action fails to establish a *prima facie* case of obviousness regarding either claim 5 or claim 6. Consequently, Applicant respectfully requests reversal of each rejection of claims 5 and 6.

3. Enablement of References

Claim 5 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". Applicant respectfully submits that neither Webb nor Boone enable a "single chip program execution device" that comprises the limitations of claim 5. Consequently, Applicant respectfully requests reversal of the rejection of claim 5 and the rejection of claim 6, which is dependent upon claim 5.

4. Legally Insufficient Suggestion or Motivation to Combine Webb with Boone

The present Office Action presents a legally insufficient suggestion or motivation to combine Webb with Boone. Regarding this combination, the present Office Action asserts, at

page 4:

> [b]ased on Webb's CPU paradigm, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Webb's CPU in a single-chip as taught by Boone because this single-chip would incorporate in one monolithic structure programmable and alterable control logic and storage thereof and processing and control functionalities, thus providing flexible possibilities for code customization while minimizing connections that would otherwise be required to implement all the interfacing pertinent to said functionalities (*see* Boone: col. 1 line 36 to col. 2, line 57).

As an initial matter, applicant points out that Boone has only a "ROM". Accordingly, the calculator of Boone could not "incorporate in one monolithic structure programmable and **alterable** control logic and **storage** thereof" as asserted by the present Office Action. Moreover, Applicant respectfully asks where does this relied upon portion of Boone provide one skilled in the art with any suggestion or motivation to:

a.) "select the references"?

b.) "select the teachings of [the] separate references"?

c.) "combine [those teachings] in the way that would produce the claimed invention"?

Applicant respectfully submits that the relied upon portion of Boone does not provide a legally sufficient suggestion or motivation to combine Boone with Webb. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 5 and 6.

G. Claims 7 and 8

1. Missing Elements

Claim 7, upon which claim 8 depends, recites *inter alia*, yet the applied portions of Webb fail to teach, "said binary programmable logic control program comprising **a compilation of a symbolic user program combined with a system support kernel to form a single executable module.**" The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where

does Webb teach, "said binary programmable logic control program comprising a compilation of a symbolic user program combined with a system support kernel to form a single executable module"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not overcome the deficiencies of Webb.

Thus, even if there were motivation or suggestion to modify or combine the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the applied references (another assumption with which the applicant disagrees), the combined applied references still do not expressly or inherently teach or suggest every limitation of claims 7 or 8. Consequently, Applicant respectfully requests reversal of the rejection of claims 7 and 8.

2. An Inoperative Combination Would Result From Combining Webb with Boone

Claim 7 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". In order to overcome the deficiencies of Webb, the present Office Action proposes a combination with Boone. Yet claim 7 recites *inter alia*, "a re-programmable read only memory" into which "said binary programmable logic control program" is loaded. Webb requires a random access or reprogrammable memory to store, *inter alia*, "the ladder logic program", "information needed to carry out the user program", "the status of discrete input and output devices", "the preset and accumulated values of counters and timers", "internal I/O relay equivalents", "timer status" values, "counter status" values, and "numerical data". See at least page 32 of Webb. However, the calculator of Boone only comprises ROM memory. See e.g., ROM 208 of FIG. 2. Regarding this memory, Boone allegedly recites **"programmable read only memory** and the programmable logic arrays **are easily modified by changing only the gate-insulator mask for the metal-insulator-semiconductor integrated system embodiment during the fabrication process."** See col. 2, lines 6-11.

Applicant respectfully submits that placing the single chip "calculator" of Boone in the "programmable logic controller" of Webb would result in a device that would be inoperative for programmable logic controller functionality due to a lack of either random access memory or reprogrammable memory.

Accordingly, Applicant respectfully submits "[i]t is inappropriate to combine" Webb and Boone since the combination "would produce a seemingly inoperative device." Accordingly, the present Office Action fails to establish a *prima facie* case of obviousness regarding claim 7. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 7 and 8.

3. Enablement of References

Claim 7 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". Applicant respectfully submits that neither Webb nor Boone enable a "single chip program execution device" that comprises the limitations of claim 7. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 7 and 8.

4. Legally Insufficient Suggestion or Motivation to Combine Webb with Boone

The present Office Action presents a legally insufficient suggestion or motivation to combine Webb with Boone. Regarding this combination, the present Office Action asserts, at page 4:

> [b]ased on Webb's CPU paradigm, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Webb's CPU in a single-chip as taught by Boone because this single-chip would incorporate in one monolithic structure programmable and alterable control logic and storage thereof and processing and control functionalities, thus providing flexible possibilities for code customization while minimizing connections that would otherwise be required to implement all the interfacing pertinent to said functionalities (see Boone: col. 1 line 36 to col. 2, line 57).

As an initial matter, applicant points out that Boone has only a "ROM". Accordingly, the calculator of Boone could not "incorporate in one monolithic structure programmable and **alterable** control logic and **storage** thereof" as asserted by the present Office Action. Moreover, Applicant respectfully asks where does this relied upon portion of Boone provide one skilled in the art with any suggestion or motivation to:

a.) "select the references"?

b.) "select the teachings of [the] separate references"?

c.) "combine [those teachings] in the way that would produce the claimed invention"?

Applicant respectfully submits that the relied upon portion of Boone does not provide a legally sufficient suggestion or motivation to combine Boone with Webb. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 7 and 8.

H. Claims 9 and 10

1. Missing Elements

Claim 9, upon which claim 10 depends, recites *inter alia*, yet the applied portions of Webb fail to teach, "**a compilation of a user program and a system support kernel.**" The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach, "**a compilation of a user program and a system support kernel**"?

Claim 9, upon which claim 10 depends, recites *inter alia*, yet the applied portions of Webb fail to teach, "said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module." The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach, "said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not overcome the deficiencies of Webb.

Thus, even if there were motivation or suggestion to modify or combine the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the applied references (another assumption with which the applicant disagrees), the combined applied references still do not

expressly or inherently teach or suggest every limitation of claims 9 or 10. Consequently, Applicant respectfully requests reversal of the rejection of claims 9 and 10.

2. An Inoperative Combination Would Result From Combining Webb with Boone

Claim 9 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". In order to overcome the deficiencies of Webb, the present Office Action proposes a combination with Boone. Yet claim 9 recites *inter alia*, "a re-programmable read only memory" into which "said binary programmable logic control program" is stored. Webb requires a random access or reprogrammable memory to store, *inter alia*, "the ladder logic program", "information needed to carry out the user program", "the status of discrete input and output devices", "the preset and accumulated values of counters and timers", "internal I/O relay equivalents", "timer status" values, "counter status" values, and "numerical data". See at least page 32 of Webb. However, the calculator of Boone only comprises ROM memory. See e.g., ROM 208 of FIG. 2. Regarding this memory, Boone allegedly recites "**programmable read only memory** and the programmable logic arrays **are** easily **modified by changing only the gate-insulator mask for the metal-insulator-semiconductor integrated system embodiment during the fabrication process.**" See col. 2, lines 6-11.

Applicant respectfully submits that placing the single chip "calculator" of Boone in the "programmable logic controller" of Webb would result in a device that would be inoperative for programmable logic controller functionality due to a lack of either random access memory or reprogrammable memory.

Accordingly, Applicant respectfully submits "[i]t is inappropriate to combine" Webb and Boone since the combination "would produce a seemingly inoperative device." Accordingly, the present Office Action fails to establish a *prima facie* case of obviousness regarding claim 9. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 9 and 10.

3. Enablement of References

Claim 9 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". Applicant respectfully submits that neither Webb nor

Boone enable a "single chip program execution device" that comprises the limitations of claim 9. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 9 and 10.

4. Legally Insufficient Suggestion or Motivation to Combine Webb with Boone

The present Office Action presents a legally insufficient suggestion or motivation to combine Webb with Boone. Regarding this combination, the present Office Action asserts, at page 4:

> [b]ased on Webb's CPU paradigm, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Webb's CPU in a single-chip as taught by Boone because this single-chip would incorporate in one monolithic structure programmable and alterable control logic and storage thereof and processing and control functionalities, thus providing flexible possibilities for code customization while minimizing connections that would otherwise be required to implement all the interfacing pertinent to said functionalities (see Boone: col. 1 line 36 to col. 2, line 57).

As an initial matter, applicant points out that Boone has only a "ROM". Accordingly, the calculator of Boone could not "incorporate in one monolithic structure programmable and **alterable** control logic and **storage** thereof" as asserted by the present Office Action. Moreover, Applicant respectfully asks where does this relied upon portion of Boone provide one skilled in the art with any suggestion or motivation to:

a.) "select the references"?

b.) "select the teachings of [the] separate references"?

c.) "combine [those teachings] in the way that would produce the claimed invention"?

Applicant respectfully submits that the relied upon portion of Boone does not provide a legally sufficient suggestion or motivation to combine Boone with Webb. Consequently, Applicant respectfully requests reversal of the rejection of each of claims 9 and 10.

I. Claim 11

1. Missing Elements

Claim 11, upon which claim 6 depends, recites *inter alia*, yet the applied portions of Webb fail to teach, "said binary programmable logic control program comprising a binary module derived via compiling a symbolic user program, **the binary module combined with a system support kernel to form a single executable module.**" The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach, "said binary programmable logic control program comprising a binary module derived via compiling a symbolic user program, **the binary module combined with a system support kernel to form a single executable module**"?

Claim 11 recites, *inter alia*, yet the applied portions of Webb fail to teach, "**compiling,** at said communication/programming device, **said symbolic user program with a system support kernel to form said binary programmable logic control program.**" The present Office Action alleges that this claimed subject matter is present in Webb at "ch. 3-2, 3-3, pg. 42-47; ch. 18-3, 18-4, pg. 259-266; Fig. 2-3; table 2-4 – pg. 30". Yet these applied portions of Webb do not even mention a "system support kernel". Thus Applicant respectfully asks how and where does Webb teach, "**compiling**, at said communication/programming device, **said symbolic user program with a system support kernel to form said binary programmable logic control program**"?

Applicant respectfully submits that this claimed subject matter is not present in Webb. The applied portions of Boone do not overcome the deficiencies of Webb.

Thus, even if there were motivation or suggestion to modify or combine the applied references (an assumption with which the applicant disagrees), and even if there were a reasonable expectation of success in combining or modify the applied references (another assumption with which the applicant disagrees), the combined applied references still do not expressly or inherently teach or suggest every limitation of claim 11. Consequently, Applicant respectfully requests reversal of the rejection of claim 11.

2. An Inoperative Combination Would Result From Combining Webb with Boone

Claim 11 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". In order to overcome the deficiencies of Webb, the present Office Action proposes a combination with Boone. Yet claim 9 recites *inter alia*, "a re-programmable read only memory" within which "said binary programmable logic control program" is stored. Webb requires a random access or reprogrammable memory to store, *inter alia*, "the ladder logic program", "information needed to carry out the user program", "the status of discrete input and output devices", "the preset and accumulated values of counters and timers", "internal I/O relay equivalents", "timer status" values, "counter status" values, and "numerical data". See at least page 32 of Webb. However, the calculator of Boone only comprises ROM memory. See e.g., ROM 208 of FIG. 2. Regarding this memory, Boone allegedly recites "**programmable read only memory** and the programmable logic arrays **are** easily **modified by changing only the gate-insulator mask for the metal-insulator-semiconductor integrated system embodiment during the fabrication process.**" See col. 2, lines 6-11.

Applicant respectfully submits that placing the single chip "calculator" of Boone in the "programmable logic controller" of Webb would result in a device that would be inoperative for programmable logic controller functionality due to a lack of either random access memory or reprogrammable memory.

Accordingly, Applicant respectfully submits "[i]t is inappropriate to combine" Webb and Boone since the combination "would produce a seemingly inoperative device." Accordingly, the present Office Action fails to establish a *prima facie* case of obviousness regarding claim 11. Consequently, Applicant respectfully requests reversal of the rejection of claim 11.

3. Enablement of References

Claim 11 recites *inter alia*, and the present Office Action admits that Webb does not teach, "a single chip program execution device". Applicant respectfully submits that neither Webb nor Boone enable a "single chip program execution device" that comprises the limitations of claim 11. Consequently, Applicant respectfully requests reversal of the rejection of claim 11.

4. Legally Insufficient Suggestion or Motivation to Combine Webb with Boone

The present Office Action presents a legally insufficient suggestion or motivation to combine Webb with Boone. Regarding this combination, the present Office Action asserts, at page 4:

> [b]ased on Webb's CPU paradigm, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement Webb's CPU in a single-chip as taught by Boone because this single-chip would incorporate in one monolithic structure programmable and alterable control logic and storage thereof and processing and control functionalities, thus providing flexible possibilities for code customization while minimizing connections that would otherwise be required to implement all the interfacing pertinent to said functionalities (see Boone: col. 1 line 36 to col. 2, line 57).

As an initial matter, applicant points out that Boone has only a "ROM". Accordingly, the calculator of Boone could not "incorporate in one monolithic structure programmable and **alterable** control logic and **storage** thereof" as asserted by the present Office Action. Moreover, Applicant respectfully asks where does this relied upon portion of Boone provide one skilled in the art with any suggestion or motivation to:

a.) "select the references"?

b.) "select the teachings of [the] separate references"?

c.) "combine [those teachings] in the way that would produce the claimed invention"?

Applicant respectfully submits that the relied upon portion of Boone does not provide a legally sufficient suggestion or motivation to combine Boone with Webb. Consequently, Applicant respectfully requests reversal of the rejection of claims 11.

VIII. CLAIMS APPENDIX

Appendix A sets forth all pending claims in the state in which they were appealed.

IX. EVIDENCE APPENDICES

Appendix B sets forth copies of evidence submitted pursuant to 37 CFR 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner.

X. RELATED PROCEEDINGS APPENDIX

Appendix C sets forth copies of decisions rendered by a court or the Board in all related proceedings.

PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

SUMMARY

In view of the above, Applicant submits that all claims on appeal distinguish over the applied art and respectfully request that the rejections of these claims should be reversed.

Applicant therefore respectfully requests that the Board of Patent Appeals and Interferences reverse the decision rejecting claims 4-11 and direct that the application be passed to issue.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 19-2179. The Examiner is invited to contact the undersigned at 434-972-9988 to discuss any matter regarding this application.

Respectfully submitted,

Michael Haynes PLC

Michael N. Haynes

Date: 12 June 2006

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PATENT

Application # 09/697,419

Attorney Docket # 1999P07938US01 (1009-045)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Alan D. McNutt
Serial No.	:	09/697,419
Filed	:	26 October 2000
Application Title	:	RE-PROGRAMMABLE FLASH MEMORY MICRO CONTROLLER AS PROGRAMMABLE LOGIC CONTROLLER
Art Unit #	:	2124
Examiner	:	Tuan A. Vu
Docket No.	:	1999P07938US01 (1009-045)

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P.O. Box 1450
Alexandria, VA 22313-1450

APPENDIX A

1. – 3. (cancelled)

4. An apparatus comprising:

a programmable logic controller lacking instructions to convert a user program from a symbolic form to a binary form, said programmable logic controller comprising:

a single chip program execution device comprising:

a micro controller operable to implement programmable logic controller I/O functions upon executing a compilation comprising the user program and a system support kernel, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program; and

a re-programmable read only memory within which the compilation is stored, said single chip program execution device separable from a

communication/programming device adapted to convert the user program to a binary code module and combine the binary code module with the system support kernel into a single executable firmware module, said programmable logic controller lacking a memory device external to said single chip program execution device.

5. A method comprising:

receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and

compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program.

6. The method of claim 5, comprising:

providing said binary programmable logic control program to said single chip program execution device.

7. A method comprising:

receiving, from a communication/programming device, a binary programmable logic control program at a single chip program execution device having a re-programmable read only memory, said communication/programming device separable from said single chip program execution device, said binary programmable logic control program comprising a compilation of a symbolic user program combined with a system support kernel to form a single executable module, the system support kernel adapted to provide a programmable logic controller with operating system functions comprising sequencing the user program, said single chip program execution device adapted to

execute said binary programmable logic control program to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and

loading said binary programmable logic control program into said re-programmable read only memory of said program single chip execution device.

8. The method of claim 7, further comprising:

executing said binary programmable logic control program on a micro controller of said single chip program execution device.

9. A programmable logic controller system, comprising:

within a single chip, a program execution device having a re-programmable memory, said program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program comprising a compilation of a user program and a system support kernel, said binary programmable logic control program adapted to operate a programmable logic controller, said programmable logic controller lacking a memory device external to said single chip program execution device; and

a communication/programming device separable from said program execution device, said communication/programming device providing functions required for external communication of said binary programmable logic control program, said binary programmable logic control program comprising a binary module formed from compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said communication/programming device adapted to load said binary programmable logic control program into said re-programmable memory and wherein said binary programmable logic control program is stored in said re-programmable memory of said program execution device by direct manipulation of logic controls of said re-programmable memory.

10. The programmable logic controller system according to claim 9, further comprising:

a watchdog timer.

11. A machine-readable medium storing instructions for activities comprising:

receiving a symbolic user program at a communication/programming device, said communication/programming device separable from a single chip program execution device having a re-programmable read only memory, said single chip program execution device adapted to execute a binary programmable logic control program, said binary programmable logic control program stored within said re-programmable memory, said binary programmable logic control program adapted to operate a programmable logic controller, said binary programmable logic control program comprising a binary module derived via compiling a symbolic user program, the binary module combined with a system support kernel to form a single executable module, the system support kernel adapted to provide said programmable logic controller with operating system functions comprising sequencing the user program, said programmable logic controller lacking a memory device external to said single chip program execution device; and

compiling, at said communication/programming device, said symbolic user program with a system support kernel to form said binary programmable logic control program.

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PATENT

Application # 09/697,419

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APPENDIX B

No evidence appendices are presented.

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APPENDIX C

There are no decisions in any related proceedings.

PAGE 32/32 * RCVD AT 6/12/2006 10:36:24 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/16 * DNIS:2738300 * CSID:Sent via MaxEmail * DURATION (mm-ss):09-12